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PATENT
Docket No. INTEL/17225

**IN THE UNITED STATES PATENT
AND TRADEMARK OFFICE**

| | | |
|---------------------------------|---|--|
| Applicants: |) | I hereby certify that this paper and the |
| |) | documents referred to as enclosed |
| TIAN et al. |) | therewith are being deposited with the |
| |) | United States Postal Service as first |
| U.S. Serial No.: 10/677,414 |) | class mail, postage prepaid, in an |
| |) | envelope addressed to Commissioner |
| For: "Methods and Apparatus for |) | for Patents, P.O. Box 1450, |
| Reducing Memory Latency |) | Alexandria, Virginia 22313-1450 on |
| in a Software Application" |) | this date: |
| |) | |
| Filed: October 2, 2003 |) | October 14, 2004 |
| |) | |
| Assignee: Intel Corporation |) |  |
| |) | |
| Group Art Unit: 2121 |) | Mark C. Zimmerman |
| |) | Attorney for Applicant(s) |
| Examiner: Not Yet Assigned |) | Registration No. 44,006 |

STATUS LETTER

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

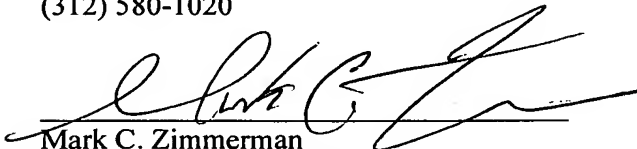
Kindly advise when an Office action can be expected in the above-referenced matter.

Respectfully submitted,

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Chicago, Illinois 60606
(312) 580-1020

October 14, 2004

By:


Mark C. Zimmerman
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Attorneys for Intel Corporation